

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Wayne A. Britson et al.  
Serial No. : 10/733,693  
Filed : December 11, 2003  
For : METHODS AND APPARATUS FOR TESTING AN IC  
Examiner : Samir Wadie Rizk  
Group Art Unit : 2112

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450


**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Sir:

Applicants respectfully request a review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reasons stated on the attached sheets.

Respectfully Submitted,

Dated: November 8, 2007  
Tarrytown, New York

  
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**ATTACHMENT TO PRE-APPEAL BRIEF REQUEST FOR REVIEW****THE REJECTIONS ARE CLEARLY NOT PROPER AND ARE WITHOUT BASIS**

In the Final Office Action (dated August 8, 2007), claims 1-4, 6, 8, and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,894,708 to *Watari* (hereinafter "*Watari*") in view of U.S. Patent No. 6,961,347 to *Bunton et al.* (hereinafter "*Bunton*"). The rejection of claim 1 is illustrative as to how the rejections are clearly not proper and are without basis.

Claim 1 is directed to a method for testing an integrated circuit (IC), comprising, *inter alia*:

if the test result is unsuccessful,  
performing at least one of:

selecting and automatically switching to a  
remaining one of the plurality of input lines  
to receive the test signal for the processor  
using a first selection signal; and

selecting and automatically switching to a  
remaining one of the plurality of output  
lines to send the test result from the  
processor using a second selection signal.

The Examiner expressly admits that "*Watari* does not teach" the above-referenced features and instead relies on *Bunton*. *Final Office Action*, pages 3-4, lines 17-13. In short, the Applicants respectfully submit that *Bunton* simply does not disclose or even relate to input or output lines to receive or send test signals for/from a processor. Further, the citation does not mention selecting and automatically switching based on selection signals.

*Bunton* does not relate to input or output lines to receive or send test signals for/from a processor. Instead, *Bunton* discusses channels in network environments.

Specifically, the cited section of *Bunton* discloses different combinations for Infinibands and not processor test lines.

Additionally, the Applicants respectfully submit that the citation does not mention selecting and automatically switching based on selection signals. Rather, *Bunton* discusses sending training data sets from a transmit port to a receive port, and using this process to correct lane errors. The Applicants respectfully submit that this discussion does not teach or suggest selecting and automatically switching based on selection signals.

For at least the above-reasons, the Applicants respectfully submit that neither *Watari* nor *Bunton*, individually or combined, may be relied upon for teaching or suggesting the above-recited features of claim 1.

#### CONCLUSION

The Proposed combination of references relied upon in rejecting the claims under 35 U.S.C. § 103 does not teach or suggest every feature of the claims. Accordingly, the Applicants respectfully submit that the Examiner's rejections are clearly not proper, without basis, and should be withdrawn. Further, the Applicants respectfully request that the Office issue a finding that the application is allowed on the existing claims and the prosecution is closed.

Respectfully Submitted,



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